Claims

1. A bandgap voltage reference circuit including an amplifier having first and second input nodes, and providing a reference voltage at an output thereof, the circuit additionally including at least two pairs of transistors, each pair having a first transistor adapted to operate at a different current density to that of a second transistor of the pair, such that, in use, a difference in base emitter voltages, ΔV_{be}, between the two transistors of each pairing is generated and wherein the pairs are arranged such that those transistors having a first current density are provided in a chain coupled to the first input node and those transistors having the second current density are provided in a chain coupled to the second input node, the combination of the ΔV_{be} provided by each pairing contributing to an enhanced ΔV_{be} at the output of the amplifier, the enhanced ΔV_{be} being generated across a resistor provided at the output of the amplifier.

2. The circuit of claim 1 wherein three pairs of transistors are provided, each of the pairs contributing a ΔV_{be} component, such that the enhanced ΔV_{be} generated across the resistor at the output of the amplifier is equivalent to $3\Delta V_{be}$.

3. The circuit as claimed in claim 2 being further adapted to generate a curvature correction voltage by driving each of the three transistors operating at the first current density with a Proportional to Absolute Temperature (PTAT) current and the other three transistors with a constant current, the sum of the curvature correction voltage and the $3\Delta V_{be}$ being both applied across the resistor on the output of the amplifier, thereby correcting for curvature associated with the bandgap circuit, and providing a temperature insensitive voltage reference output.

4. The circuit as claimed in claim 3 wherein the PTAT current is generated by mirroring the current defined across the resistor on the output of the amplifier so as to drive each of the transistors operating at the first current density.

5. The circuit as claimed in claim 1 wherein each of the transistors are provided in a MOS process implementation.

6. The circuit as claimed in claim 2 wherein two of the pairs of transistors are formed using bipolar transistors and the third pair is formed using lateral transistors.

7. The circuit as claimed in claim 6 wherein the third pair provides an input stage of the amplifier.

8. The circuit as claimed in claim 7 wherein the third pair provides an asymmetric input stage of the amplifier.

9. The circuit as claimed in claim 7 further including a pair of load transistors coupled to the third pair of transistors, the load transistors being adapted to equalise the currents through the third pair of transistors.

10. The circuit as claimed in claim 7 wherein the third pair of transistors are both driven with a PTAT current.

11. The circuit as claimed in claim 10 wherein the PTAT current provided is generated externally to the circuit.

12. The circuit as claimed in claim 9 wherein a second stage of the amplifier is provided by a MOS transistor which is driven by a PTAT current source, the MOS transistor being coupled to one of the load transistors and the collector of one of the transistors forming the third pair of transistors.

13. The circuit as claimed in claim 1 further including a MOS transistor provided at the output of the amplifier, the MOS transistor being driven with a PTAT current, the base of the MOS transistor being coupled directly to the output node of the amplifier and the emitter node providing an output of the circuit.

14. The circuit as claimed in claim 13 wherein the source of the MOS transistor is coupled to the emitter of a bipolar transistor, the collector of the bipolar transistor is coupled to a reference potential, and the base of the bipolar transistor is coupled to the resistor.

15. The circuit as claimed in claim 2 wherein each of the three pairs of transistors are provided in a bipolar configuration, the third pair providing an input stage of an amplifier, the amplifier having an output node coupled to a bipolar transistor provided in a voltage follower configuration, and wherein the voltage reference is provided at a node between the output of the amplifier and the voltage follower.

16. The circuit as claimed in claim 2 being further adapted to provide at the output of the amplifier a voltage indicative of the temperature as sensed on the circuit, thereby providing a temperature sensor, the voltage indicative of the temperature being effected by driving each of the first and second chains of transistors with a Proportional to Absolute Temperature (PTAT) current, the $3\Delta V_{be}$ being applied across the resistor on the output of the amplifier, thereby providing at an output node a voltage indicative of the temperature on the device.

17. A bandgap voltage reference circuit adapted to provide at an output thereof a reference voltage, the reference voltage being provided by the combination of generated Complimentary to Absolute Temperature (CTAT) and PTAT voltages, the CTAT voltage being provided by a base emitter voltage of a forward biased transistor and the PTAT voltage being provided by multiple ΔV_{be} voltages, each ΔV_{be} voltage being generated by a pair of bipolar transistors operating at different current densities, the PTAT voltage being solely defined by a current applied across a single resistor provided at an output of an amplifier.

18. A bandgap voltage reference circuit having an amplifier with a first and second input node and providing at an output thereof a reference voltage, each input node being coupled to a chain of at least two transistors, the transistors being arranged such that the emitter of a first transistor is coupled to the base of

a second transistor, the emitter of the second transistor being coupled to the input of the amplifier and the collectors of each transistor being coupled to a reference potential and wherein those transistors in a first chain are adapted to operate at a first current density and those transistors in a second chain are adapted to operate at a second different current density, such that a difference in base emitter voltages between transistors in the first and second chain is provided, the difference being equivalent to a multiple ΔV_{be} and being generated by the current provided across a sole load resistor coupled to the output of the amplifier.

19. A temperature reference circuit including an amplifier having at its non-inverting input node at least one bipolar transistor operable at a first current density and in a feedback loop between the output of the amplifier and its inverting input node, at least one bipolar transistor operable at a second current density lower then that of the transistor coupled to the non-inverting input, such that due to the difference in current density of the transistors coupled to each of the two inputs a ΔV_{be} is reflected at the output of the amplifier and wherein the transistors coupled to each of the input nodes of the amplifier are driven with PTAT currents such that the ΔV_{be} voltage developed is temperature sensitive, thereby providing a voltage reference circuit adapted to provide a measurement of temperature.

20. The circuit as claimed in claim 19 wherein two or more transistors are provided in a stack arrangement coupled to each of the input nodes of the amplifier, the difference in current density between the transistors in each stack generating an enhanced ΔV_{be} at the output of the amplifier.

21. The circuit as claimed in claim 19 wherein the PTAT currents are generated externally to the circuit.

22. The circuit as claimed in claim 19 wherein the PTAT currents are generated internally within the circuit, the ΔV_{be} being developed across a sole resistor coupled between the output of the amplifier and a reference potential.

23. The circuit as claimed in claim 20 wherein the enhanced ΔV_{be} is developed as a PTAT voltage across a sole resistor coupled between the output of the amplifier and a reference potential.